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06/13/00 jc852 U.S. PTO

UTILITY PATENT APPLICATION TRANSMITTAL
(Large Entity)

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Docket No.
1920/106

Total Pages in this Submission
28

jc498 U.S. PTO 09/592813 06/13/00

TO THE ASSISTANT COMMISSIONER FOR PATENTS
Box Patent Application
Washington, D.C. 20231

Transmitted herewith for filing under 35 U.S.C. 111(a) and 37 C.F.R. 1.53(b) is a new utility patent application for an invention entitled:

PASSIVE BALUN FET MIXER

and invented by:

Philip Piro
Kevin Cornman

If a CONTINUATION APPLICATION, *check appropriate box and supply the requisite information:*

☐ **Continuation** ☐ **Divisional** ☐ **Continuation-in-part (CIP)** of prior application No.: _____

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Enclosed are:

Application Elements

1. ☐ Filing fee as calculated and transmitted as described below

2. ☒ Specification having **14** pages and including the following:

   a. ☒ Descriptive Title of the Invention
   b. ☒ Cross References to Related Applications *(if applicable)*
   c. ☐ Statement Regarding Federally-sponsored Research/Development *(if applicable)*
   d. ☐ Reference to Microfiche Appendix *(if applicable)*
   e. ☒ Background of the Invention
   f. ☒ Brief Summary of the Invention
   g. ☒ Brief Description of the Drawings *(if drawings filed)*
   h. ☒ Detailed Description
   i. ☒ Claim(s) as Classified Below
   j. ☒ Abstract of the Disclosure

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Application Elements (Continued)

3. ☒ Drawing(s) *(when necessary as prescribed by 35 USC 113)*
   - a. ☐ Formal Number of Sheets _____
   - b. ☒ Informal Number of Sheets 7
4. ☒ Oath or Declaration
   - a. Newly executed *(original or copy)* ☒ Unexecuted
   - b. ☐ Copy from a prior application (37 CFR 1.63(d)) *(for continuation/divisional application only)*
   - c. ☒ With Power of Attorney ☐ Without Power of Attorney
   - d. ☐ *DELETION OF INVENTOR(S)*
     Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. 1.63(d)(2) and 1.33(b).
5. ☐ Incorporation By Reference *(usable if Box 4b is checked)*
   The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. ☐ Computer Program in Microfiche *(Appendix)*
7. ☐ Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all must be included)*
   - a. ☐ Paper Copy
   - b. ☐ Computer Readable Copy *(identical to computer copy)*
   - c. ☐ Statement Verifying Identical Paper and Computer Readable Copy

Accompanying Application Parts

8. ☐ Assignment Papers *(cover sheet & document(s))*
9. ☐ 37 CFR 3.73(B) Statement *(when there is an assignee)*
10. ☐ English Translation Document *(if applicable)*
11. ☐ Information Disclosure Statement/PTO-1449 ☐ Copies of IDS Citations
12. ☐ Preliminary Amendment
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Accompanying Application Parts (Continued)

15. ☐ Certified Copy of Priority Document(s) *(if foreign priority is claimed)*

16. ☐ Additional Enclosures *(please identify below):*

Fee Calculation and Transmittal

CLAIMS AS FILED

For	#Filed	#Allowed	#Extra		Rate	Fee
Total Claims	17	- 20 =	0	x	$18.00	$0.00
Indep. Claims	3	- 3 =	0	x	$78.00	$0.00
Multiple Dependent Claims (check if applicable) ☐						$0.00
					BASIC FEE	$690.00
OTHER FEE ***(specify purpose)***						
					TOTAL FILING FEE	$690.00

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John J Stickevers
Signature

Dated: **June 13, 2000**

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CERTIFICATE OF MAILING BY "EXPRESS MAIL" (37 CFR 1.10) Applicant(s): **Piro et al.**			Docket No. **1920/106**
Serial No. **Not Yet Assigned**	Filing Date **Herewith**	Examiner **Not Yet Assigned**	Group Art Unit **Not Yet Assigned**

Invention: **PASSIVE BALUN FET MIXER**

I hereby certify that this **Utility Patent Application with documents referenced therein**
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application for

PASSIVE BALUN FET MIXER

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1920/106

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PASSIVE BALUN FET MIXER

Priority

This application claims priority from U.S. provisional application serial number 60/139,679 filed June 16, 1999, entitled "Passive Balun FET Mixer" which is incorporated herein, by reference.

Technical Field

The present invention relates to mixer circuits, of the type having inputs for local oscillator (LO) and radio frequency (RF) signals and an intermediate frequency (IF) output, and in particular to mixer circuits using field effect transistors (FETs).

Background Art

Mixers are contained in many radio transmitters, receivers, and other communication devices. Such mixers operate by combining an RF signal with LO, a periodic signal, producing a mixed output. This mixed output contains signals whose frequencies consist of either the sum or difference between RF and LO frequencies. By filtering the mixed output, an IF signal can be created whose frequency is either higher or lower than the original RF frequency.

As a result of the desire to decrease the size of communication devices, mixer size must also be reduced. Double balanced diode mixers, widely used in the industry, are large. By utilizing FETs instead of diodes, and removing the multiple baluns, size can be reduced without sacrificing performance.

Passive floating FET mixers are known in the art. A floating FET configuration uses an electrically symmetrical FET, whose drain and source terminals float with respect to ground and are coupled to the output port via a balun, as described in Vasile, C. F., Floating GASFET Circuits Offering Unique Signal Processing from DC-EHF, 1985 GOMAC Proceedings, Pp.305-309, 1985, incorporated herein by reference in it's entirety. Fig.1, taken from Vasile's article, shows a single floating FET configuration. An alternative floating FET configuration

which replaces the single transistor with two transistors in series is shown in Fig. 2, also taken from Vasile's article. U.S. patent 4,705,967, issued for an invention of Vasile and incorporated herein by reference in it's entirety, discloses a floating multifunction FET circuit that may be used as a mixer, as shown in Fig. 3. The IF is extracted from the same side of the balun **328** as the RF signal. Therefore, the balun in this design must be large to account for both the higher frequency RF signal and the lower frequency IF signal. Additionally, the RF and IF signals are not isolated, resulting in possible distortion of these signals.

Mourant, in US. patent 5,697,092 and in "A Low cost Mixer for Wireless Applications," 1995 IEEE Microwave Systems Conference pp. 21-24, also discloses similar subject matter pertaining to passive floating FET mixers, each of which is hereby incorporated herein by reference in its entirety. In U.S. patent 5,697,092, a single, floating FET mixer suitable for compact construction is disclosed, as shown in Fig. 2, taken from Mourant. The balanced IF created in the FET mixer is extracted at the RF balun in an unbalanced manner, being diplexed from the balun center tap. A series inductor **414** and capacitor **415** resonates at the RF frequency and shorts out center tap **412** to ground **406**. At low frequencies, the capacitor is an open, allowing the IF **416** to be extracted. The balun is fabricated with primary and secondary windings consisting of planar metal spirals that are interleaved with one another, as described by Mourant, col. 4, lines 11-18. One problem with this design is that adding a centertap to a balun adds steps to the manufacturing process. Additionally, the centertap position must be located, requiring calculation and testing. Another problem is that the IF output leads must cross over portions of the interleaved windings, making it susceptible to parasitic capacitance.

Summary of the Invention

In accordance with one aspect of the invention, a FET mixer uses a balun having a primary and secondary, with the primary coupled to an RF signal input. The mixer also includes a pair of field effect transistors (FETs), wherein the gates are coupled to one another and to a local oscillator input. One of the source and the

drain of the second of the two transistors is coupled at a node to one of the source and the drain of the other of the two transistors, and the node is coupled to ground. The other of the source and the drain of the first of the two transistors is coupled to one side of the secondary of the balun and the other of the source and the drain of the second of the two transistors is coupled to the other side of the secondary of the balun. An intermediate frequency signal output is coupled to a point in the circuit path between the first and second transistors.

In a further related embodiment, at the node, one of the source and the drain of the second of the two transistors is connected to ground, and the node is coupled to one of the source and drain of the first of the two transistors by means of a filter. In a related embodiment, the filter has a capacitor serving as a shunt at the frequency of the RF signal but not at the frequency of the intermediate frequency signal.

In another related embodiment, the local oscillator input is coupled to the gates via a capacitor so as to cause the transistors to be biased near pinch off, and a capacitance is disposed across the balun secondary to tune the secondary. The capacitance may optionally be realized by a pair of capacitors connected in series, wherein the node at a connection between the capacitors is coupled to ground. Also optionally, the secondary has a center tap, and the center tap is coupled to ground.

In accordance with another aspect of the invention, a method of mixing a periodic signal and a radio frequency signal producing an intermediate frequency signal is provided. A radio frequency signal is applied to a primary of a balun. Simultaneously, a periodic signal is applied to a first and a second switch, each switch coupled to the other switch and also coupled to a secondary of the balun, resulting in a frequency translation of the periodic signal and the radio frequency signal producing a mixed output. The intermediate frequency signal is outputted by filtering the mixed output between the first and second switch. In a further related embodiment, the filter includes coupling one switch at a node to ground, and coupling the other switch to the node by means of a filter. The filter may apply a

capacitance that serves as a shunt at the frequency of the RF signal but not at the frequency of the intermediate signal. In another related embodiment, a capacitance is applied across the balun primary to tune the primary. A capacitance may optionally be applied across the balun secondary to tune the secondary, which may include a pair of capacitors in series, wherein the node at a connection between the capacitors is coupled to ground. In another related embodiment, ground is coupled to the center tap of the balun secondary.

In another embodiment, a FET mixer uses a transformer, having a primary and secondary, the primary coupled to an RF signal. The mixer also has a pair of switches, comprising of a first switch and a second switch, wherein the gates of the switches are coupled to one another and to a periodic signal input. The first switch is coupled at a node to ground, and the node is coupled to the second switch. Additionally, one switch is attached to one side of the secondary of the transformer, and the other switch is attached to the other side of the secondary of the transformer. An intermediate frequency signal output is coupled to a point in the circuit path between the first and second transistor. In a further related embodiment, at the node, one of the switches is connected to ground, and the node is coupled to the other switch by means of a filter. The filter may have a capacitor that serves as a shunt at the frequency of the RF signal but not at the frequency of the intermediate frequency signal. In another related embodiment, tuning circuitry is disposed across the transformer's secondary, and may include a pair capacitors in series, wherein the node at a connection between the capacitors is coupled to ground. In another related embodiment, the secondary of the transformer has a center tap, which is coupled to ground. In another related embodiment, tuning circuitry is disposed across the primary of the transformer.

Brief Description of the Drawings

The foregoing features of the invention will be more readily understood by reference to the following detailed description, taken with reference to the accompanying drawings, in which:

Fig. 1a shows a prior art single floating FET configuration, as shown in U.S. patent 4,705,967.

Fig. 2 shows a prior art series connected floating FET configuration, as shown in U.S. patent 4,705,967.

Fig. 3 is a schematic view of a prior art single FET mixer, as shown in U.S. patent 4,705,967.

Fig. 4 is a schematic view of a prior art single FET mixer, as shown in U.S. patent 5,697,092.

Fig. 5 is a block diagram of a passive balun FET mixer in accordance with an embodiment of the present invention.

Fig. 6 is a schematic view of a passive balun FET mixer in accordance with an embodiment of the present invention.

Fig. 7 is a schematic view of a minimum configuration of the passive balun FET mixer in accordance with an embodiment of the present invention.

Fig. 8 is a flowchart depicting a method of mixing a periodic signal and a radio frequency signal producing an intermediate frequency.

Detailed Description of Specific Embodiments

For the purposes of the description herein and the claims that follow it, unless the context otherwise requires, the term "Radio Frequency" (RF) means an electromagnetic signal at frequencies in the range extending from below 3 kilohertz to 300 gigahertz, which includes radio and television transmission. These frequencies are above audio signals and below the frequencies of visible light. The term "intermediate frequency" (IF) shall mean the frequency that an incoming signal is changed to. The term "local oscillator" (LO) shall mean a periodic signal. The term "balun" shall mean a transformer connected between a balanced source or load and an unbalanced source or load. A balanced line has two conductors, with equal currents in opposite directions. The unbalanced line has just one conductor; the current in it returns via a common ground or earth path.

Fig. 5 is a block diagram of the passive balun FET mixer in accordance with

an embodiment of the present invention. Two switches **506, 508** are turned on and off by a periodic signal **502**. An RF signal **516** is applied to the primary of a transformer **514**, which is coupled to the balanced side of the balun across the switches. A frequency translation of the periodic signal and the RF signal is thus produced. The IF signal is retrieved by applying a filter **510** to the mixed output between the first and second switch, as opposed to extracting the IF signal from the centertap of the transformer. By not utilizing the centertap of the balun to extract the IF, several benefits are achieved. The manufacturing process is simplified, the centertap position does not have to be found and tested, and a potential source of parasitic capacitance is removed. Optional tuning circuitry **512** for the primary and secondary of the transformer may be added, along with biasing circuitry **504**.

Fig. 6 shows a passive balun FET mixer in accordance with another embodiment of the present invention. The mixer includes two FET transistors, Q1 and Q2. The drains of Q1 and Q2 are connected to the secondary winding of a transformer TX1 acting as a balun. A coupling capacitor C1 couples a local oscillator (LO) input to the gates of Q1 and Q2. The mixer also includes an IF bypass capacitor C2, and three tuning capacitors C3, C4, and C5.

The gates of the two FETs are connected together and coupled to the LO signal by a capacitor C1. The use of two FETs allows each transistor to handle less voltage, creating less distortion in FET output. Additionally, the parasitic capacitances formed across the gates of each transistor to LO will cancel as a result of using two FETs.

The primary winding of the transformer TX1 is coupled between the RF input port and ground. One side of the secondary winding of the transformer TX1 is connected to the drain of FET transistor Q1, and the other side of the secondary winding of transformer TX1 is connected to the drain of Q2. The source of transistor Q2 is connected to ground, while the source terminal of transistor Q1 is coupled to ground through capacitor C2. Capacitor C2, as discussed below, is at RF frequencies the equivalent of a short circuit. Therefore at RF frequencies, the sources of Q1 and

Q2 are at ground potential, and thus neither Q1 nor Q2 is a floating FET.

A tuning capacitor C5 is placed across the terminals of the primary winding of TX1. Capacitors C3 and C4 tune the secondary winding. Capacitors C3 and C4 may optionally be replaced by a single capacitor in shunt across the secondary of TX1, with the risk that the signals on Q1 and Q2 may be less balanced.

The seconclary may be optionally center-tapped as shown in Fig. 6. The midpoint of the secondary is coupled to ground through capacitor C6 in order to provide better symmetry in the RF signal at the drains of transistors Q1 and Q2. If the center tap is not used, then capacitor C6 is not necessary.

Capacitor C1 allows for passive self-biasing of the FETs near pinch-off voltage due to rectification of the positive half cycle of LO voltage. As a result, no external biasing is required. Capacitor C1 is charged with the gate side at a negative potential relative to the LO side of the capacitor. Then on the negative half cycle, the lower LO voltage in combination with the charge on C1 keeps each FET from conducting. The LO signal modulates the channel resistance of the FETs from a minimum value when Vgs is approximately zero volts to a maximum value at voltage less than -Vpinch off. The time-varying resistances of the channels of Q1 and Q2 terminate the RF circuit, which includes the transformer TX1 and tuning capacitors C3, C4, and C5. These time-varying resistances, which vary at the rate of the LO frequency, effect the conversion of the RF signal to new signals at frequencies that equal the sums and differences of the LO and RF frequencies and their integer multiples.

The signal corresponding to the difference between the LO and RF frequency is known as the intermediate frequency (IF). The IF signal is conveniently retrieved between transistors Q1 and Q2, instead of at the centertap of the balun. Capacitor C2 acts as a low pass filter to reject higher frequency signals and to allow only the IF to pass through to the IF output.

Fig. 7 shows a minimum configuration of the passive balun FET mixer shown in fig. 6, in accordance with an embodiment of the present invention. Optional

tuning capacitors C3, C4, and C5 capacitors and coupling capacitor C1 have been removed. The mixer includes two FET transistors, Q1 and Q2. The drains of Q1 and Q2 are connected to the secondary winding of a transformer TX1 acting as a balun. The mixer also includes the IF bypass capacitor C2.

Fig. 8 shows a method of mixing a periodic signal and a radio frequency signal producing an intermediate frequency. RF is applied to a primary of a balun **(step 804)**, isolating RF from the balun secondary. A periodic signal is applied to a first and second switch, each switch coupled to the other switch, and also attached to a secondary of the balun **(step 806)**. The periodic signal simultaneously turns on and off each transistor periodically, resulting in multiplication of the RF and periodic signals. A mixed signal is thus created, consisting of frequencies equal to the sum and difference of the RF and periodic signal frequencies. A filter is applied to the mixed output between the first and second switch to obtain the intermediate frequency **(step 808)**. Utilizing a low pass filter, the higher frequency component of the mixed signal is shunted to ground, resulting in down-frequency translation of the RF signal. Alternatively, utilizing a high pass filter will result in up-frequency translation of the RF signal.

In one embodiment of the present invention, the passive balun FET mixer is operable at RF frequencies in the multi-gigahertz range, although this invention will operate in other RF ranges. At these multi-gigahertz frequencies, capacitances are typically in the approximate range of 1-20 pF, with capacitor C2 being of the order of 15 pF, and all other capacitances less than 5 pF. The FETs Q1 and Q2 may be realized as Metal-Semiconductor Field Effect Transistors (MESFETs), which are FETs fabricated of gallium arsenide (GaAs) and formed with a metal-semiconductor junction. The use of MESFETs is not intended to limit the scope of the invention and other types of FETs may be used.

Although various exemplary embodiments of the invention have been disclosed, it should be apparent to those skilled in the art that various changes and modifications can be made which will achieve some of the advantages of the

invention without departing from the true scope of the invention. These and other obvious modifications are intended to be covered by the claims that follow.

What is claimed is:

1. A field effect transistor mixer comprising:

a. a balun having a primary and a secondary, the primary coupled to a radio frequency signal input;

b. a pair of field effect transistors, each transistor having a gate, a source, a drain, and a channel between the source and the drain, wherein

i. the gates of the transistors are coupled to one another and to a local oscillator input,

ii. one of the source and the drain of a first of the two transistors is coupled at a node to one of the source and the drain of the other of the two transistors, and the node is coupled to ground,

iii. the other of the source and the drain of the first of the two transistors is coupled to one side of the secondary of the balun and the other of the source and the drain of the second of the two transistors is coupled to the other side of the secondary of the balun;

c. and an intermediate frequency signal output coupled to a point in the circuit path between the first and second transistors.

2. A mixer according to claim 1, wherein, at the node, one of the source and the drain of the second of the two transistors is connected to ground, and the node is coupled to one of the source and drain of the first of the two transistors by a filter.

3. A mixer according to claim 2, the filter having a capacitor serving as a shunt at the frequency of the Radio frequency signal but not at the frequency of the intermediate frequency signal.

4. A mixer according to claim 1, wherein the local oscillator input is coupled to the gates via a capacitor so as to cause the transistors to be biased near pinch off.

5. A mixer according to claim 1, further comprising a capacitance disposed across the balun secondary to tune the secondary.

6. A mixer according to claim 5, wherein the capacitance includes a pair of capacitors connected in series, wherein the node at a connection between the capacitors is coupled to ground.

7. A mixer according to claim 1, wherein the secondary has a center tap, and the center tap is coupled to ground.

8. A method of mixing a periodic signal and a radio frequency signal producing an intermediate frequency signal, the method comprising:

applying the radio frequency signal to a primary of a balun;

applying a periodic signal simultaneously to a first and a second switch, each switch coupled to the other switch and also coupled to a secondary of the balun, resulting in a frequency translation of the periodic signal and the radio frequency signal producing a mixed output; and

outputting the intermediate frequency signal by filtering the mixed output between the first and second switch.

9. A method according to claim 8, wherein the step of outputting the intermediate signal by filtering the output between the first and second switch includes coupling one switch at a node to ground, and coupling the other switch to the node by a filter.

10. A method according to claim 8, wherein the step of filtering of the mixed output includes applying a capacitance that serves as a shunt at the frequency of the Radio frequency signal but not at the frequency of the intermediate signal.

11. A method according to claim 8, further comprising applying a capacitance across the balun primary to tune the primary.

12. A method according to claim 8, further comprising applying a capacitance across the balun secondary to tune the secondary.

13. A method according to claim 12, wherein the capacitance includes a pair of capacitors in series, wherein the node at a connection between the capacitors is coupled to ground.

14. A method according to claim 8, further comprising coupling ground to the center tap of the balun secondary.

15. A field effect transistor Mixer comprising:

a. a transformer having a primary and a secondary, the primary coupled to a Radio frequency signal;

b. a pair of switches, comprising of a first switch and a second switch, wherein

i. the gates of the switches are coupled to one another and to a periodic signal input,

ii. the first switch is coupled at a node to ground, and the node is coupled to the second switch,

iii. one switch is attached to one side of the secondary of the transformer, and the other switch is attached to the other side of the secondary of the transformer; and

c. an intermediate frequency signal output coupled to a point in the circuit path between the first and second transistors.

16. A mixer according to claim 15, wherein, at the node, one of the switches is connected to ground, and the node is coupled to the other switch by a filter.

17. A mixer according to claim 16, the filter having a capacitor serving as a shunt at the frequency of the Radio frequency signal but not at the frequency of the intermediate frequency signal.

18. A mixer according to claim 15, further comprising tuning circuitry disposed across the transformer's secondary.

19. A mixer according to claim 15, wherein the secondary of the transformer has a center tap, and the center tap is coupled to ground.

20. A mixer according to claim 15, further comprising tuning circuitry disposed across the primary of the transformer.

Attorney Docket: 1920/106

PASSIVE BALUN FET MIXER

Abstract

A FET mixer uses a balun having a primary and secondary, with the primary coupled to an Radio frequency signal input. The mixer also includes a pair of field effect transistors (FETs), wherein the gates are coupled to one another and to a local oscillator input. One of the source and the drain of the second of the two transistors is coupled at a node to one of the source and the drain of the other of the two transistors, and the node is coupled to ground. The other of the source and the drain of the first of the two transistors is coupled to one side of the secondary of the balun and the other of the source and the drain of the second of the two transistors is coupled to the other side of the secondary of the balun. An intermediate frequency signal output is coupled to a point in the circuit path between the first and second transistors.

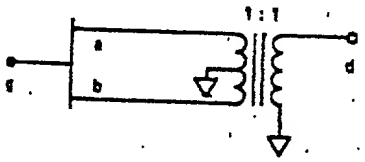

Fig. 1 SIMPLEST FF CIRCUIT USING AN IDEAL BALUN

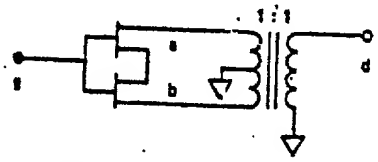

Fig. 2 SERIES CONNECTED FF

Prior Art

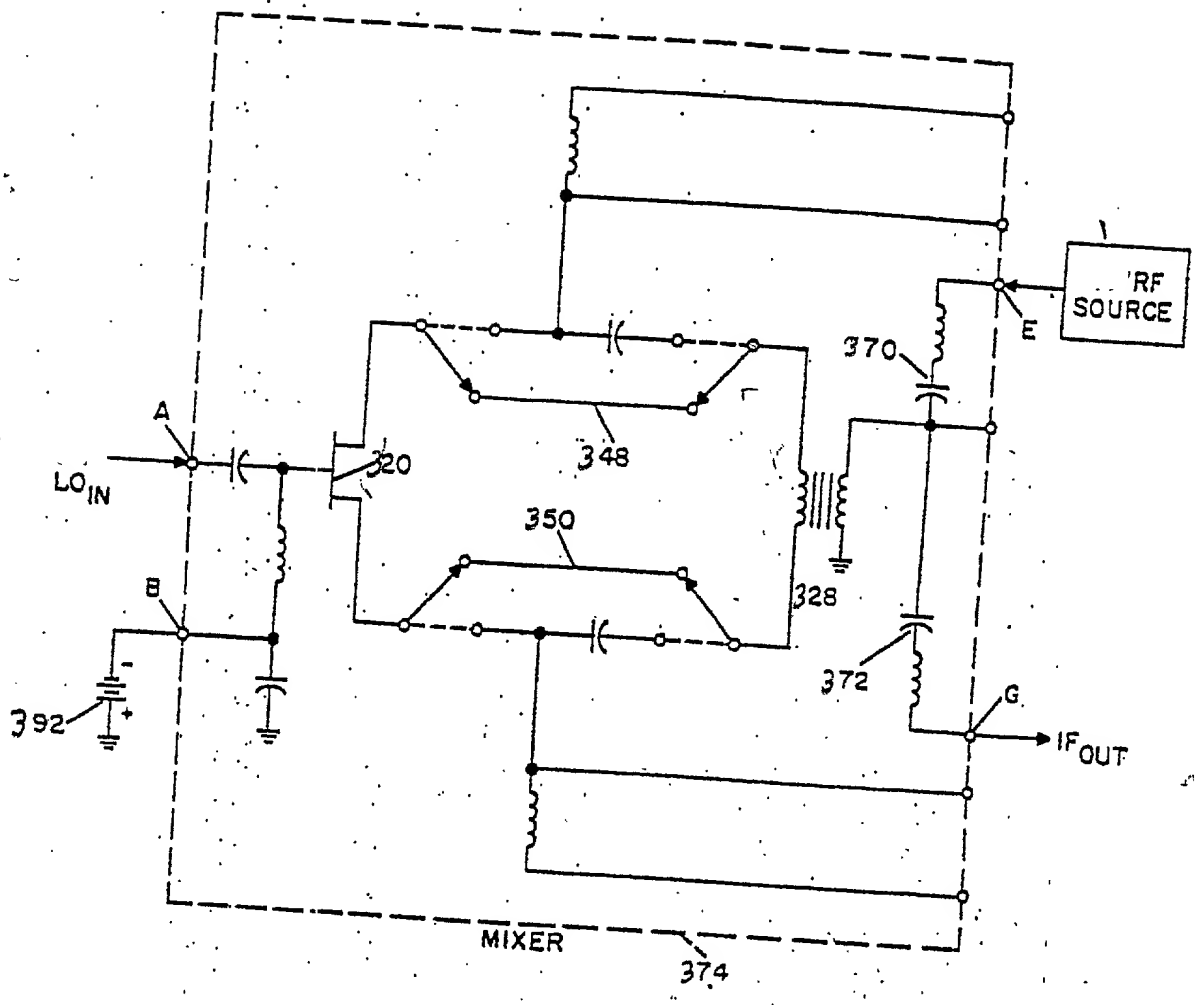

Fig. 3
Prior Art

Figure 4
Prior Art

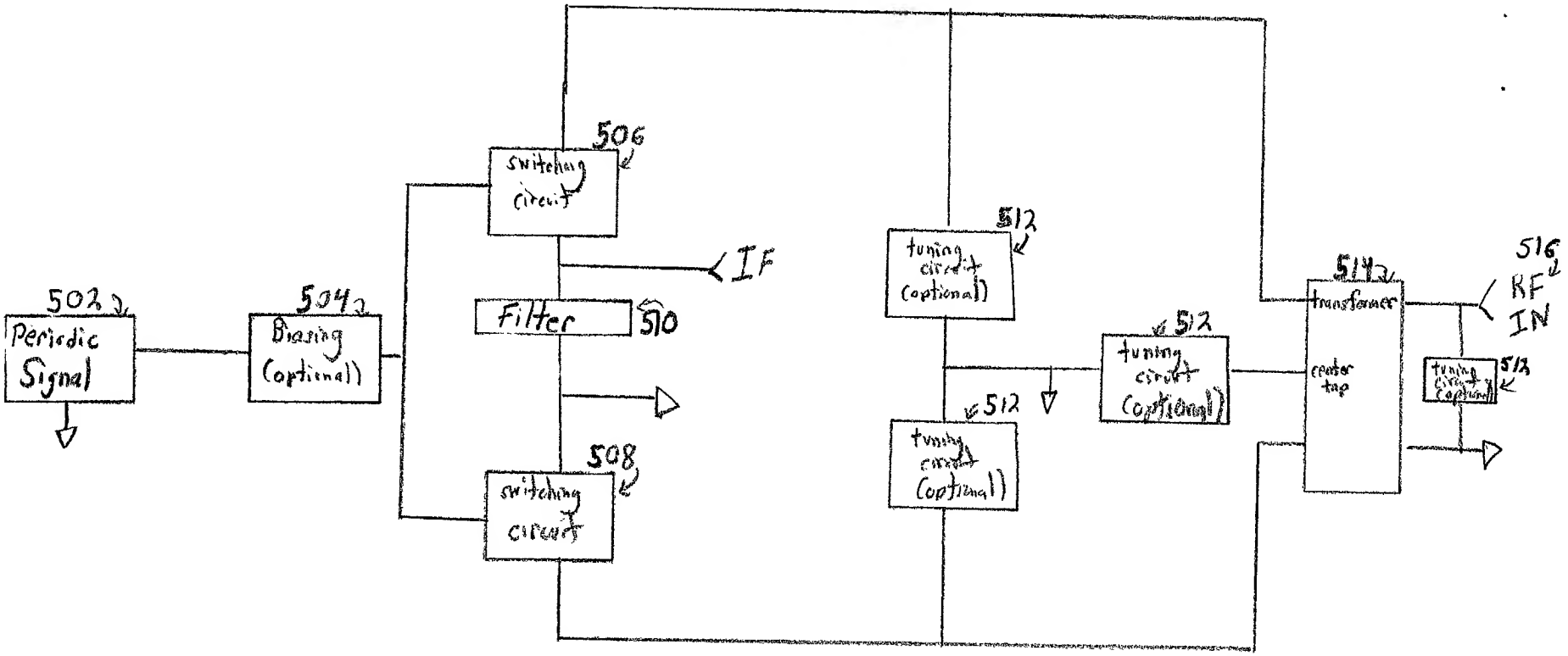
502
Periodic Signal
504
Biasing (optional)
506
switching circuit
IF
Filter
510
508
switching circuit
512
tuning circuit (optional)
512
tuning circuit (optional)
512
tuning circuit (optional)
514
transformer
center tap
516
RF IN
512
tuning circuit (optional)

Figure 5

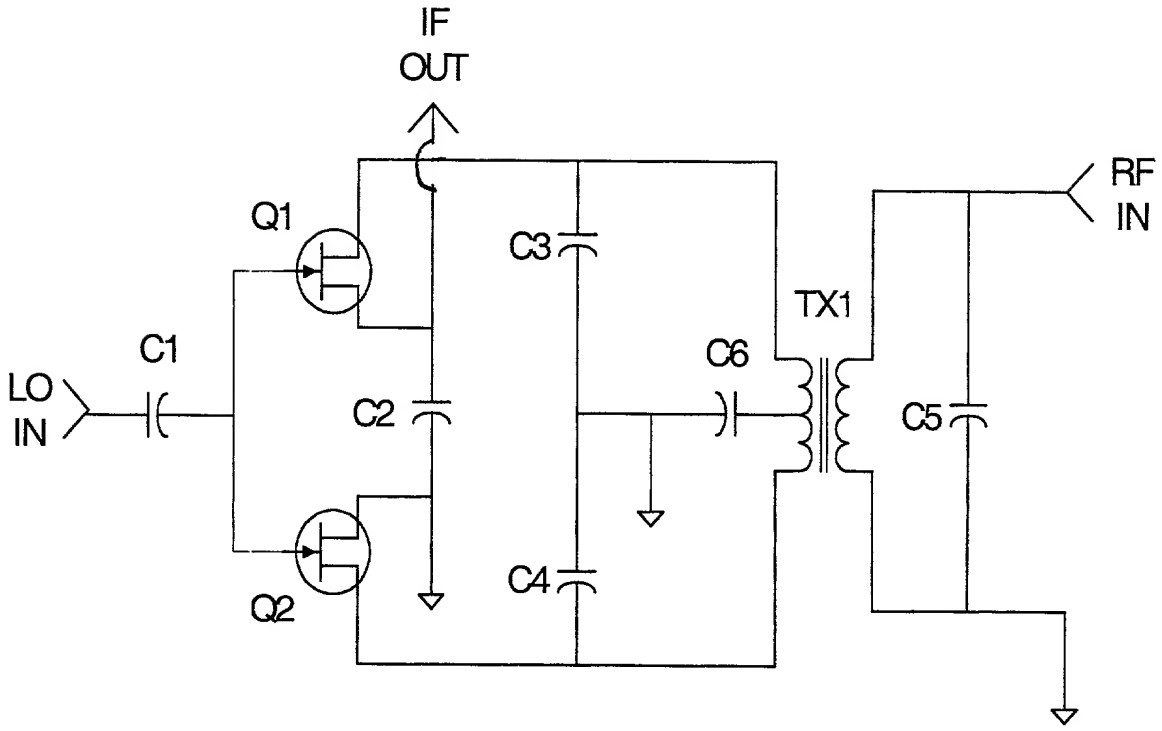

Figure 6

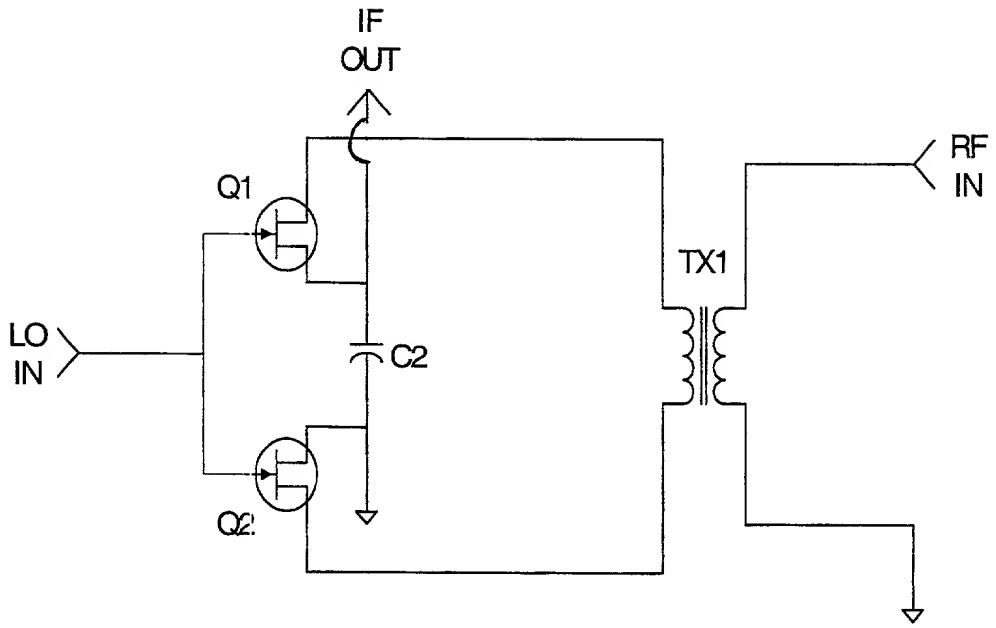

Figure 7

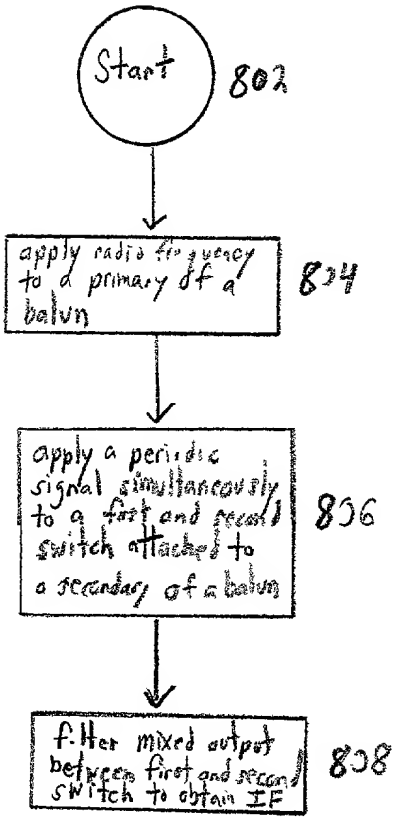
Start
802
apply radio frequency to a primary of a balun
804
apply a periodic signal simultaneously to a first and second switch attached to a secondary of a balun
806
filter mixed output between first and second switch to obtain IF
808

Figure 8

Docket No.
1920/106

Declaration and Power of Attorney For Patent Application

English Language Declaration

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

PASSIVE BALUN FET MIXER

the specification of which

(check one)

☒ is attached hereto.

☐ was filed on _____ as United States Application No. or PCT International Application Number _____

and was amended on _____

(if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d) or Section 365(b) of any foreign application(s) for patent or inventor's certificate, or Section 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)			Priority Not Claimed
_____ (Number)	_____ (Country)	_____ (Day/Month/Year Filed)	☐
_____ (Number)	_____ (Country)	_____ (Day/Month/Year Filed)	☐
_____ (Number)	_____ (Country)	_____ (Day/Month/Year Filed)	☐

I hereby claim the benefit under 35 U.S.C. Section 119(e) of any United States provisional application(s) listed below:

(Application Serial No.)	(Filing Date)
60/139,679	June 16, 1999

I hereby claim the benefit under 35 U. S. C. Section 120 of any United States application(s), or Section 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. Section 112, I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, C. F. R., Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application:

(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. *(list name and registration number)*

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